DUAL CELL MEMORY DEVICE HAVING A TOP DIELECTRIC STACK

ABSTRACT OF THE DISCLOSURE

A non-volatile memory device includes a semiconductor substrate and a pair of buried bitlines within the substrate. A bottom dielectric layer is formed over the substrate and a charge trapping dielectric layer is formed over the bottom dielectric layer. A multi-layer top dielectric stack is formed over the charge trapping dielectric layer. The top dielectric stack includes a first oxide layer, a nitride layer, and a second oxide layer. A wordline is formed over the top dielectric stack. The multi-layer top dielectric stack has a reduced electrical thickness, thereby providing a memory device, which is operative to be programmed using a reduced operating voltage of less than about +8 Volts.